ID: P2.19

Title: Molecular-Dynamics Study of Crack-Fracture Mechanism by Stealth Dicing

Name: Shimamura, Kohei

Affiliation: Kumamoto University

The process of cutting a wafer into individual IC chips is performed in semiconductor manufacture, which is called 'dicing'. Recently, an innovative dicing method, called 'Stealth Dicing(SD)', has been developed by Hamamatsu Photonics K.K. In the SD, a permeable nanosecond laser pulse is focused inside the wafer. Due to the pulse energy accumulation, the crystalline structure of the irradiated area is modified. By applying a tensile strain the wafer is diced into chips. In this process, cracks are considered to be initiated in the irradiated region and grow to the surface. It is a great advantage that the wafer surface has no damage, while the interior is modified. However, their microscopic details are still unknown. For this purpose, we have carried out computer simulations based on the molecular-dynamics method. The laser-induced processes have been studied using several model systems consisting of millions of silicon atoms with the Stillinger-Weber potential. We have found that, in the area irradiated by the laser, the temperature rises rapidly, and melting occurs. In such area, a large density fluctuation occurs accompanying with the thermal fluctuation. When the irradiation ends, atoms are condensed into an amorphous state, which has a higher density than the crystal. As a result, voids are generated in the laser-irradiated region. However, amorphous silicon is unstable, and recrystallization must occur eventually. We have seen that the recrystallization takes place at the boundary between the amorphous and crystalline phases. It should be emphasized that the voids remain even after the recrystallization process is stopped being in agreement with the experiments. This fact means that the density of the laser-irradiated region increases in proportion to the volume of the voids. We will also discuss the details of the stress distribution around the laser-irradiated region inside the wafer and the void-formation process.